NASA SBIR 2021 Phase I Solicitation

Z2.02   High-Performance Space Computing Technology

Lead Center: JPL

Participating Center(s): GSFC

Scope Title:

High-Performance Space Computing Technology

Scope Description:

Most current NASA missions utilize 20-year-old space computing technology that is inadequate for future missions. Newer processors with improved performance are becoming available from industry but still lack the performance, power efficiency, and flexibility needed by the most demanding mission applications. The NASA High-Performance Spaceflight Computing (HPSC) project is addressing these needs. This subtopic solicits technologies that can enable future high-performance, multicore processors, along with the supporting technologies needed to fully implement avionics systems based on these processors.

- Runtime system software security: Software support to enable secure boot, signed applications, and runtime system monitoring is needed to ensure the integrity of onboard, real-time computing systems.
- Compilers that support software-implemented fault tolerance (SIFT) capabilities (e.g., control flow checking, coordinated checkpoint/rollback, recovery block) for multicore processors are desired.
- Technologies are needed to enable radiation-tolerant and fault-tolerant onboard networks with >10 Gbps bandwidth per lane, including intellectual property (IP) cores for endpoints and switches, software stack, and verification and test tools.
- A fault-tolerant RISC-V processor IP core is needed that is augmented to provide data parallelism, which is needed to accelerate image processing and science data processing.
- Solid-state data recorders are needed that are suitable for operation in the space

environment, support the space extensions to Serial Rapid IO, and have redundant interfaces.

Expected TRL or TRL Range at completion of the Project: 4 to 6
Primary Technology Taxonomy:
Level 1: TX 02 Flight Computing and Avionics
Level 2: TX 02.X Other Flight Computing and Avionics
Desired Deliverables of Phase I and Phase II:

- Analysis
- Prototype
- Hardware
- Software

Desired Deliverables Description:

Phase I Deliverables:

For software and hardware elements, a solid conceptual design, plan for full-scale prototyping, and simulations and testing results to justify prototyping approach. Detailed specifications for intended Phase II deliverables.

Phase II Deliverables:

For software and hardware elements, a prototype that demonstrates sufficient performance and capability and is ready for future development and commercialization.

State of the Art and Critical Gaps:

Most NASA missions utilize processors with in-space qualifiable high-performance computing that has high power dissipation (approximately 18 W), and the current state of practice in Technology Readiness Level 9 (TRL-9) space computing solutions have relatively low performance (between 2 and 200 DMIPS (Dhrystone million instructions per second) at 100 MHz). A recently developed radiation-hardened processor provides 5.6 GOPS (giga operations per second) performance with a power dissipation of 17 W. Neither of these systems provide the performance, the power-to-performance ratio, or the flexibility in configuration, performance, power management, fault tolerance, or extensibility with respect to heterogeneous processor elements. Onboard network standards exist that can provide >10 Gbps bandwidth, but not everything is available to fully implement them.

Relevance / Science Traceability:

The HPSC ecosystem is enhancing to most major programs in the Human Exploration and Operations Mission Directorate (HEOMD). It is also enabling for key Space Technology Mission Directorate (STMD) technologies that are needed by HEOMD, including the Safe and Precise Landing - Integrated Capabilities Evolution (SPLICE) project. Within the Science Mission Directorate (SMD), strong mission pull exists to enable onboard autonomy across Earth science, astrophysics, heliophysics, and planetary science missions. There is also relevance to other high-bandwidth processing applications within SMD, including adaptive optics for astrophysics missions and science data reduction for hyperspectral Earth science missions.

References:

RISC-V: https://riscv.org/news/2019/09/risc-v-gains-momentum-as-industry-demands-custom-processors-for-new-innovative-workloads/

Next Generation Space Interconnect
Standard: http://www.rapidio.org/wp-content/uploads/2014/10/RapidIO-NGSIS-Seminar-July-23-2014.pdf

He, J. et al. Provably Correct Systems. Formal Techniques in Real-Time and Fault-Tolerant Systems. pp 288-335. ProCoS. 1994.

Reis, G.A. SWIFT: software implemented fault tolerance. International Symposium on Code Generation and Optimization. IEEE. 2004.

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