



NASA SBIR 2020 Phase I Solicitation

22.02 High Performance Space Computing Technology

Lead Center: JPL

Participating Center(s): GSFC

Technology Area: TA11 Modeling, Simulation, Information Technology and Processing

Scope Title

Avionics Computing Support

Scope Description

The NASA State-Of-the-Art (SOA) in space computing utilizes 20-year-old technology and is inadequate for future missions. In conjunction with the United States Air Force (USAF), NASA is investing in the development of the High-Performance Spaceflight Computing (HPSC) Chiplet, a radiation-hardened multi-core processor that will improve space computing capabilities by two orders of magnitude. Another joint NASA-USAF project will develop rad-hard, high capacity, high-speed memory components that will likewise improve space computing capabilities by approximately two orders of magnitude. And yet another project, with a planned start date of FY 2019, will start developing a single board computer based on an HPSC-chiplet.

While these efforts will provide an underlying platform, they do not provide the full range of advanced computing capabilities that will be required to support missions currently in the planning stage for the mid-2020s and beyond. Topics of interest include:

- HPSC-compatible Coprocessors: General purpose neural networks and other machine learning accelerators for robotic vision, system health management, and similar applications are needed to meet performance: power requirements in future autonomous robotic systems. Initial design of this application-specific integrated circuit (ASIC) and a validated field-programmable gate arrays (FPGA) implementation of critical portions of the design is desired. A successful SBIR will potentially lead to a Phase 3 award, or alternate funding, to implement the final chiplet.
- Fault Tolerant, Real Time Linux: A flight qualifiable version of Linux for the HPSC Chiplet, capable of supporting parallel and heterogeneous processing for autonomy, robotics and science codes is desired. Initial design of a verifiably reliable, fault tolerant, real time Linux kernel is desired. A successful SBIR will potentially result in a Phase 3 award, or alternate funding, to develop a complete, qualified, operating system.
- Compilers that support Software Implemented Fault Tolerance (SIFT) capabilities (e.g., control flow checking, coordinated checkpoint/rollback, recovery block) for the HPSC Chiplet is desired. A successful SBIR will potentially result in a Phase 3 award, or alternate funding, to implement a complete SIFT-capable software development system.

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- Fault tolerant middleware to Support HPSC Chiptlet Parallel Processing: Includes math and I/O libraries to support robotic capabilities, autonomy and science processing, and including library routines for Neon Single instruction, Multiple Data (SIMD) processors as well as A53 general purpose processors.
 - Technology and languages to enable development of provably correct software.
 - Radiation tolerant standard cell libraries for processes below 28nm that are suitable for NASA missions in the natural space environment.

NASA has plans to purchase services for delivery of payloads to the Moon through the Commercial Lunar Payload Services (CLPS) contract. Under this subtopic, proposals may include efforts to develop payloads for flight demonstration of relevant technologies in the lunar environment. The CLPS payload accommodations will vary depending on the particular service provider and mission characteristics. Additional information on the CLPS program and providers can be found at this link: <https://www.nasa.gov/content/commercial-lunar-payload-services>. CLPS missions will typically carry multiple payloads for multiple customers. Smaller, simpler, and more self-sufficient payloads are more easily accommodated and would be more likely to be considered for a NASA-sponsored flight opportunity. Commercial payload delivery services may begin as early as 2020 and flight opportunities are expected to continue well into the future. In future years it is expected that larger and more complex payloads will be accommodated. Selection for award under this solicitation will not guarantee selection for a lunar flight opportunity.

References

<https://www.nasa.gov/press-release/goddard/2017/nasa-selects-high-performance-spaceflight-computing-hpsc-processor-contractor>

Expected TRL or TRL range at completion of the project: 4 to 6

Desired Deliverables of Phase II

Prototype, Analysis, Hardware, Software

Desired Deliverables Description

For hardware elements, a preliminary design ready for detailed design, fabrication, and production.

State of the Art and Critical Gaps

The SOA in space qualifiable high performance computing has high power dissipation (approximately 18 W) and the SOP in TRL-9 space computing have relatively low performance (between 2 DMIPS to 200 DMIPS at 100 MHz). Neither of these systems provides the performance, power:performance ratio, or the flexibility in configuration, performance, power management, fault tolerance, or extensibility with respect to heterogeneous processor elements. The HPSC Chiptlet, currently in development, will provide significantly enhanced capabilities but, as currently defined, lacks a broad range of coprocessors and accelerators (which are supported in the architecture but not planned for implementation) as well as software elements that will be required for use in future missions. This lack of hardware and software ecosystem elements is the focus of this nomination.

Relevance / Science Traceability

HPSC ecosystem is of interest to all major programs in HEOMD (Human Exploration and Operations Mission Directorate) and SMD (Science Mission Directorate). We have had discussions with program and project managers across NASA. Immediate infusion targets include Mars Fetch Rover, WFIRST/Chronograph, Gateway, and SPLICE/Lunar Lander.