



## NASA SBIR 2020 Phase I Solicitation

### S3.08 Command, Data Handling, and Electronics

Lead Center: GSFC

Participating Center(s): JPL, LaRC, MSFC

Technology Area: TA11 Modeling, Simulation, Information Technology and Processing

#### Scope Description

NASA's space based observatories, fly-by spacecraft, orbiters, landers, and robotic and sample return missions, require robust command and control capabilities. Advances in technologies relevant to command and data handling and instrument electronics are sought to support NASA's goals and several missions and projects under development.

The 2020 subtopic goals are to develop platforms for the implementation of miniaturized highly integrated avionics and instrument electronics that:

- Are consistent with the performance requirements for NASA missions.
- Minimize required mass/volume/power as well as development cost/schedule resources.
- Can operate reliably in the expected thermal and radiation environments.

Successful proposal concepts should significantly advance the state-of-the-art. Furthermore, proposals developing hardware should indicate an understanding of the intended operating environment, including temperature and radiation. Note that environmental requirements vary significantly from mission to mission. For example, some low earth orbit missions have a total ionizing dose (TID) radiation requirement of less than 10 krad(Si), while planetary missions can have requirements well in excess of 1 Mrad(Si).

Specific technologies sought by this subtopic include:

**Fault-tolerant computing:** Processor and eco-system (ASIC & Design IP) designed to mitigate single event upsets (SEUs) and technologies are sought that implement fault tolerant computers leveraging industry standard processor instruction set architectures (ISPIAs) and interfaces. Although not limited to, there is particular interest in leveraging the reduced instruction set computer (RISC) principles of RISC-V architecture. Offerors should identify coding language of IP cores, use of architecture specific modules which would limit the ability to swap hardware chipsets, options for scaling fault tolerance, code/gate size and features versus power and speed. Offerors working application-specific integrated circuit (ASIC) efforts should identify possible foundries and their radiation tolerance processes. Offerors offering processing units should identify operating system / toolchain support. Offerors proposing design intellectual property (IP) should identify mitigation technique(s) including burdens on code development time / hardware performance and size.

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**Multiple output point of load power regulator:** This module, preferably implemented utilizing one or more controller ASICs, will source a minimum of 3 settable output voltages when provided with standard spacecraft power bus input. Output voltages shall be independently settable to any voltage between 3.3V and .9 V with efficiency of at least 95%. Regulation, noise filtering and other operational specifications should be commensurate with industry standards for space-based systems. Output current in the 10A range to handle field-programmable gate array (FPGA) core requirements. The module should provide standard spacecraft power supply features, including over voltage protection, fault tolerance, load monitoring, sequencing, synchronization, soft start and should allow control and status monitoring by a remote power system controller. Using fewer external components is also highly desirable. There is also interest in a capability to provide data over power line communication to the converter for control and monitoring functions. The offeror should determine radiation tolerance levels achievable utilizing commercially available processes and indicate, in the proposal, the radiation tolerance goals.

**High density high-reliability interconnections:** A high reliability connector or interconnect mechanism that can operate in space environments (vacuum, vibration) and deliver hundreds of signal/power connections while using as little physical board area as possible is desired. The design should handle everything from carrying power to high speed (10+ Gbps) impedance controlled connections. The design should be scalable in different sizes to accommodate fewer connections and save board space. Low insertion force is desirable. Right angle and stacking design options should be considered.

## References

For descriptions of radiation effects in electronics, the proposer may visit (<http://radhome.gsfc.nasa.gov/radhome/overview.htm>).

**Expected TRL or TRL range at completion of the project:** 3 to 5

## Desired Deliverables of Phase II

Prototype, Hardware, Software

## Desired Deliverables Description

Desired Phase 2 deliverables for fault tolerant computing architectures are IP cores / ASIC designs implemented using an appropriate hardware design language (VHDL or Verilog) that have been demonstrated as an integrated system. Any required system software should be available, preferably as open source, to provide compilers, debuggers, and operating systems to the architecture. The fault tolerance of the architecture should be demonstrated.

Desired Phase 2 deliverable for the multiple output point of load switcher is a prototype multi-output point of load regulator. The regulator should be integrated onto a test board and be performance tested under varying resistive, capacitive, and transient load conditions.

Desired Phase 2 deliverables for the high density high-reliability interconnect are prototypes of the connection system (different size, orientations, etc.). The connector should be integrated onto a test board where its performance (speed, cross talk, etc.) can be verified.

## State of the Art and Critical Gaps

There is a need for a broader range of offerings for fault tolerant computing architectures. This includes the need for viable options between performance, size (gate count) and power tradeoffs. There are currently a few sources of fault tolerant computing, and additional variety would help reduce costs for future NASA missions. Fault tolerant computing enables robust autonomous systems to be designed and implemented. Furthermore, recent commercial processor architecture developments offer improved performance and a broader array of performance options, and fault tolerant variants of these could significantly benefit NASA missions.

There are multiple output point of load converters available from commercial companies. The existing commercial parts require many external components eliminating their space savings. Commercial parts are not built on radiation tolerant processes.

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Current connectors are too large, especially for small satellites and CubeSats. As the size of the printed circuit boards has shrunk, the percent of board space being used by the I/O connectors has become unacceptable. The connectors are taking away from circuitry and sensors that could be providing additional functionality and science products. High density commercial connectors also tend to be lacking in their general ruggedness, outgassing, and ability to prevent intermittent connections in high vibration environments like orbital launches.

### **Relevance / Science Traceability**

Fault tolerant / autonomous computing architectures are relevant to increasing science return and lowering costs for missions across all Science Mission Directorate (SMD) divisions. However, the benefits are most significant for miniaturized instruments and subsystems that must operate in harsh environments. These missions include interplanetary CubeSats and smallsats, outer planets instruments, and heliophysics missions to harsh radiation environments. For these missions, the inherent fault tolerance would provide an additional level of protection on top of the radiation tolerance of the FPGA or ASIC on which the computing system is implemented. Additionally, for missions with large communication delays, the inherent fault tolerance can limit the need for ground intervention.

Multi-output point of load converters and high-density high-reliability interconnects are relevant to miniaturizing electronics. Miniaturized flight electronics allows one to fit more functionality into less volume, allowing smaller spacecraft to perform science that was previously done by larger satellites. These missions include interplanetary CubeSats and smallsats, outer planets instruments, and heliophysics missions.