



NASA SBIR 2018 Phase I Solicitation

H9.05 Transformational/Over-the-Horizon Communications Technology

Lead Center: GRC

Participating Center(s): GSFC

Technology Area: TA5 Communication and Navigation

The proposer is expected to identify new ideas, create novel solutions and execute feasibility demonstrations. Emphasis for this subtopic is on the far-term (â‰ˆ10yrs.) insofar as mission insertion and commercialization but it is expected that the proposer proves fundamental feasibility via prototyping within the normal scope of the SBIR program. The over-the-horizon communications technology development will focus research in the following areas:

- Systems optimized for energy efficiency (information bits per unit energy).
- Advanced materials; smart materials; electronics embedded in structures; functional materials; graphene-based electronics/detectors.
- Technologies that address flexible, scalable digital/optical core processing topologies to support both RF and optical communications in a single terminal.
- Nanoelectronics and nanomagnetism; quantum logic gates; single electron computing; superconducting devices; technologies to leapfrog Mooreâ€™s law.
- Quantum communications, methods for probing quantum phenomenon, methods for exploiting exotic aspects of quantum theory.
- Human/machine and brain-machine interfacing; the convergence of electronic engineering and bio-engineering; neural signal interfacing.

The research should be conducted to demonstrate theoretical and technical feasibility during the Phase I and Phase II development cycles and be able to demonstrate an evolutionary path to insertion within approximately 10 years. Delivery of a prototype of the most critically enabling element of the technology for NASA testing at the completion of the Phase II contract is expected.

Phase I deliverables shall include a final report describing theoretical analysis and prototyping concepts. The technology should have eventual commercialization potential. For Phase II consideration, the final report should include a detailed path towards Phase II prototype hardware.