



NASA SBIR 2017 Phase I Solicitation

Z6.01 High Performance Space Computing Technology

Lead Center: JPL

Participating Center(s): GSFC, JSC

Technology Area: TA11 Modeling, Simulation, Information Technology and Processing

The NASA state-of-the-art in space computing is currently lagging commercial capabilities in both the hardware and software capabilities. Presently, NASA is investing in the development of a radiation-hardened multi-core General Purpose Processor (GPP) that is scalable for a variety of space computing application.

The GPP will require additional support components and software to enable it to function as a multi-application device. Also, the GPP may not be the best approach to specific specialized applications that require niche-processing approaches. This subtopic is seeking flight-computing enhancements in the following areas:

- GPP parallel processing support libraries such as: real-time and fault-tolerant Message Passing Interface (MPI), the Vector, Signal, and Image Processing Library (VSIPL), the Fastest Fourier Transform in the West (FFTW), and other parallel I/O and math libraries.
- Computing accelerators/co-processors that will connect to the HPSC processor via the Serial Rapid I/O (SRIO) ports for supporting specific applications such as cyber-physical/robotics and autonomous systems.
- Generic I/O expander chips for a GPP that provide typical serial data communications support suitable for use in subsystems and instruments such as TIA/EIA-422, SpaceWire, SpaceFiber, MIL-STD-1553, wireless RFID-based device interfaces, and Time Triggered Ethernet (TTE)/Time-Triggered Gigabit Ethernet (TTGbE).
- Interconnect switches and end points for SRIO with integral micro-controllers, suitable for use in subsystems and instruments including components, IP for FPGA and SOC implementation and associated software.
- Low-power Graphics Processor Units and related display technologies.
- General purpose SIMD engines.
- Neuromorphic processors, especially those using >2D topologies.
- Board-support technologies, such as fault tolerant, multiple voltage, high efficiency, Point-of-Load converters, that reduce the SWaP burden of the overall computing board to permit higher system power efficiency and smaller computing system form factors.
- High Performance, low power/power manageable, fault tolerant, memory components, both volatile and non-volatile, especially those using >2D topologies and high speed, low power interfaces such as SRIO.
- Middleware that provides machine configuration management and resource allocation for GPP and extended GPP (incorporating co-processors, accelerators and expanded I/O).