NASA SBIR 2010 Phase I Solicitation

S3.01 Command, Data Handling, and Electronics

Lead Center: GSFC

Participating Center(s): ARC, JPL, JSC, LaRC

NASA’s space based observatories, fly by spacecraft, orbiters, landers, and robotic and sample return missions, require robust command and control capabilities. Advances in technologies relevant to command and data handling and instrument electronics are sought to support NASA’s goals and several missions and projects under development.

http://science.nasa.gov/search/?q=missions+under+development
http://www.nap.edu/catalog.php?record_id=10432

The subtopic goals are to: (1) develop high-performance processors and memory architectures and reliable electronic systems, (2) develop an avionics architecture that is flexible, scalable, extensible, adaptable, and reusable, and (3) develop tools technologies that can enable rapid deployment of high-reliability, high-performance onboard processing applications and interface to external sensors on flight hardware. The subtopic objective is to elicit novel architectural concepts and component technologies that are realistic and operate effectively and credibly in environments consistent with the future NASA Science missions.

Successful proposal concepts should significantly advance the state-of-the-art. Proposals should clearly (1) state what the product is; (2) identify the needs it addresses; (3) identify the improvements over the current state of the art; (4) outline the feasibility of the technical and programmatic approach; and (5) present how it could be infused into a NASA program. Furthermore, proposals should indicate an understanding of the intended operating environment, including temperature and radiation. It should be noted that environmental requirements can vary significantly from mission to mission. For example, some low earth orbit missions have a total ionizing dose (TID) radiation requirement of less than 10 kRad, while some planetary missions can have requirements well in excess of 1MRad. For descriptions of radiation effects in electronics, the proposer may visit http://radhome.gsfc.nasa.gov/radhome/background.htm. If a Phase II proposal is awarded, the combined Phase I and Phase II developments should produce a prototype that can be characterized by NASA.

The technology priorities sought are listed below.
C&DH Architectures

- High performance hardware/software processor platform capable of implementing high-throughput numerically intensive real-time applications that entail autonomous landing and guidance and control. Sensor computations. Key performance metrics must achieve 40 GOPS, 20 GMACS, and 40,000 MIPS with EDAC-protected memory, comprising 256 (TBR) MB DDR volatile for flight software execution and 256 (TBR) MB non-volatile for image storage, respectively. Standard interfaces must include Gigabit Ethernet, RS232 UART serial ports, and control interfaces to Lidar/Camera with a maximum bandwidth of up to 1 Gbps. Platform should be in 6U form factor and consume no greater than 20 W. Processor trades should be conducted to balance size, weight, power against reliability, flexibility, and performance for future space missions. Radiation hardened by design best practices, rapid development tools, and a radiation-tolerant path to space qualification are appealing features. The platform should operate, at reduced capability, during high energy cosmic rays events. Principal capabilities will encompass command generation and handling, control of safe landing system, sensor data processing and storage, and on-board memory management, optimized for acceptable performance and reliability.

- Novel, miniaturized, low-power C&DH architectures tailored to small spacecraft. Solutions must perform functions of traditional C&DH systems at a fraction of the SWAP (Size, Weight, and Power). Proposed systems should be capable of supporting typical spacecraft C&DH functions and should be radiation tolerant, and should further be compatible with Space Plug and Play (SPA) architectures, including SPA-1.

- Development system design tools that (a) take full advantage of rapid prototyping hardware-in-the-loop (HIL) environments for hybrid processing platforms, and (b) automate/accelerate the deployment of data processing and sensor interface design on flight hardware.

Discrete Components for C&DH Subsystems

- Processors - General purpose (processor chips and radiation-hardened by design synthesizable IP cores) and special purpose single-chip components (DSPs), with sustainable processing performance and power efficiency (>40,000 MIPS at >1,000 MIPS/W for general purpose processing platforms, >20 GMACs at >5 GMACs/W for computationally-intensive processing platforms), and tolerance to total dose and single-event radiation effects. Concepts must include tools required to support an integrated hardware/software development flow.

- Radiation-hardened non-volatile low power memories >100KRad.

- Radiation hardened DDR1, DDR2, and DDR3 high speed memories.

Onboard Network Architectures and Devices

- Radiation-hardened physical layer components for (copper/fiber-optic) onboard data busses (e.g., SpaceWire, Ethernet, Serial Rapid I/O, Ring Bus) speeds >1 Gb/s.

- Power distribution through onboard data network technologies.

- Wireless data network architectures and components.

- Wireless RFID housekeeping sensors and interrogation hardware.
Tunable, Scalable, Reconfigurable, Adaptive Fault-Tolerant Onboard Processing Architectures

- Technologies Enabling Use of Commercial Devices for Spaceflight Applications, including Radiation Hardened By Software (RHBS) approaches.
- Highly adaptive reconfigurable computing platforms (including hybrid DSP/FPGA/CPU architectures).
- Tools and methodologies to accelerate development of highly reliable applications on reconfigurable computing platforms.

Technologies Enabling Custom Radiation-Hardened Component Development

- Radiation-Hardened-By-Design (RHBD) cell libraries.
- Radiation-hardened Programmable Logic Devices (PLDs) and structured ASIC devices (digital and/or mixed-signal).
- Intellectual Property (IP) cores allowing the implementation of highly reliable System-On-a-Chip (SOC) devices for spacecraft subsystems or instrument electronics. Functions of interest include processors, memory interfaces, and data bus interfaces.

Novel, Ruggedized Packaging/Interconnect

- High density packaging (enclosures, printed wiring boards) enabling miniaturization.
- Novel high density and low resistance cabling, including carbon nanotube (CNT) based wiring.

Data Compression

- Ground-based high-speed data compression decoder capable of decoding coded bit stream conforming to CCSDS 122.0-B-1 Image Data Compression standard (www.ccsds.org), providing over 40 M samples/sec for up to 16-bit image data coded in an embedded bit stream. Spaceflight hardware currently exists to perform the encoding function. The requested decoder would be used for ground processing of a downlinked encoded data stream. The decoder shall not consume more than 5 watts of power at the specified speed.

Power Conversion and Distribution

- Radiation-hardened high efficiency Point-Of-Load (POL) down convertor.
- Power distribution through onboard data network technologies.