NASA SBIR 2009 Phase I Solicitation

O1.01 Coding, Modulation, and Compression

Lead Center: JPL

Participating Center(s): AFRC, ARC, GRC, GSFC

This subtopic aims to develop innovative technology in three key areas of space communications: modulation, forward error-correction (FEC) coding, and data compression. The objective is to provide the best possible trade-off of coding gain, bandwidth efficiency, complexity (mass or power), and rate-distortion, so that the total science/engineering value can be maximized while using the smallest amount of spacecraft energy possible. This will enable NASA to meet a wide range of requirements for its future space missions at near Earth, lunar, and deep space distances.

These future missions will use many link types (direct-to-Earth, TDRS relay, lander-to-orbiter relay, and short-proximity links), frequencies (S-, X-, and Ka-bands), and application-specific performance requirements (latency, complexity). The state-of-the-art in the three areas addressed by this subtopic is summarized here:

- Modulation: BPSK and QPSK for deep space, and BPSK, QPSK, SQPSK, and 8-PSK for near Earth (TDRS) applications; GMSK for bandwidth efficient applications
- Coding: CCSDS turbo codes and LDPC codes (See http://public.ccsds.org/publications/archive/131x0b1.pdf and http://public.ccsds.org/publications/archive/131x1o2e2.pdf)
- Compression: the CCSDS standard (http://public.ccsds.org/publications/archive/122x0b1c2.pdf)

Technology development is needed in the following areas:

Modulation

There is a need for the implementation and demonstration of ground receivers and flight receivers that exhibit very low implementation loss for 8-PSK and GMSK (in addition to BPSK, QPSK, and SQPSK) for operation ranges from 8 bps (emergency) through 100 Mbps (high rate Ka-band). Emphasis is placed on minimizing implementation loss (

Phase 1 tasks should target completion of a fixed-point design whose performance can be verified by simulation (in, e.g., Simulink or SPW). Phase 2 technology target is a hardware demonstration at TRL 5.

Coding

There is a need to interface a receiver as above with a high-performing LDPC decoder. Government licensing of LDPC decoding technology (Verilog source) is available. What is needed here is the development of the following:

- FPGA simulations of all 10 CCSDS LDPC codes down to a bit error rate of $1e^{-10}$ and a codeword error rate of $1e^{-9}$, and with a goal of identifying the "error floor" of each of the codes.
- Improved decoding algorithms that reduce the observed error floor. It is known that observed error floors for these codes are a characteristic of standard belief propagation (BP) decoding, and not because of the minimum distance properties of the codes. Variations of standard decoding may not be susceptible to the same trapping sets, thereby improving error floor performance. These methods include (a) optimally decoding the 4-cycles, (b) converting 4-cycles to equivalent trees, (c) BP decoding with damping, and (d) using min in place of min* in the later iterations of the decoder. These and other variations should be tested particularly on the k=1024, r=4/5 code, which is expected to exhibit the highest error floor.

The target is a finished product at TRL 5.

Data Compression

Development of a radiation-tolerant high-speed (over 100 Msamples/sec) lossless compression component conforming to CCSDS 121.0-B-1, "lossless data compression" (www.ccsds.org) allowing input dynamic range to over 24-bit/sample. Options should include user-supplied external predictor, as well as providing potential applications to hyper-spectral data by taking advantage of the spectral correlation in such data sets.

Development to TRL 5 is desired.

Research should be conducted to demonstrate technical feasibility during Phase 1 and show a path toward a Phase 2 hardware and software demonstration and deliver a demonstration unit or software package for NASA testing at the completion of the Phase 2 contract.

The proposer to this subtopic is advised that the products proposed may be included in a future small satellite flight opportunity. Please see the SMD Topic S4 on Small Satellites for details regarding those opportunities. If the proposer would like to have their proposal considered for flight in the small satellite program, the proposal should state such and recommend a pathway for that possibility.