NASA SBIR 2007 Phase I Solicitation

01.01 Coding, Modulation, and Compression

Lead Center: GSFC

Participating Center(s): GRC, JPL

Power and spectrum efficient solutions are needed for both near-Earth and deep-space science and exploration applications. Channel coding efficiency from 50% to 87%, combined with good bit-error/burst-error correction property will provide solutions to multiple missions. A high-speed, digital receiver capable of demodulating coded modulations in addition to uncoded modulations is needed for future missions. In compression, implementation of a high-speed decoder for decoding a standard embedded bit-stream offering tunable lossy compression to lossless compression is desired. Proposals are sought in the following specific areas:

Compression

High-speed decoder capable of decoding coded bit stream conforming to CCSDS 122.0-B-1 Image Data Compression standard (www.ccsds.org) is solicited. The decoder has to provide over 640 Mbits/sec decoding for up to 16-bit image data coded in an embedded bit stream. The implementation technology shall point to potential space-use feasibility.

Coding

1. Special emphasis is placed on a channel coding design suitable for near-Earth missions, operating at least at over 80% coding rate with an error floor lower than Bit-Error-Rate (BER) of $10^{-10}$, and at least 8-bit burst-error correction property, with encoder/decoder complexity consistent with implementations at data rates close to 1 Gbps and power consumption smaller than a few watts. The new design when compared with current CCSDS Reed-Solomon (255,223) coder at BER of $10^{-5}$ shall have over 2dB Eb/No gain. The preferred code block frame length is from 4K to 16K bits. Proposed implementation technology shall point to potential space-use feasibility.
2. High-speed FPGA decoder for a set of 10 recently proposed low-density parity-check (LDPC) codes specified in a CCSDS Orange Book CCSDS 131.1-O-1 (www.ccsds.org). These codes include 9 codes, of rates 1/2, 2/3, and 4/5 and input blocklengths 1024, 4096, and 16384, and a rate 7/8 code of input blocklength 7136. The design should be capable of switching in real-time between decoders for any of the 10 codes, and have a throughput of at least 50 Mbps. There may be opportunities to use partial, stand-alone FPGA solutions developed by NASA.

**High-Rate Receiver**

High-rate receiver capable of decoding coded and un-coded modulation suite (8-PSK, GMSK, filtered OQPSK) specified by CCSDS 413.0-G-1 April 2003 (www.ccsds.org) and 16-PSK, 16-QAM, 16-APSK with processing throughput greater than 300 Mbits/sec is desired. A desirable feature for the receiver output is 7 bits/sample that can be used as input to channel decoding algorithms based on soft-decision decoding.