NASA SBIR 2007 Phase I Solicitation

O1.05 Reconfigurable/Reprogrammable Communication Systems

Lead Center: GRC

Participating Center(s): GSFC, JPL, JSC

NASA seeks novel approaches in reconfigurable, reprogrammable communication systems to enable the Vision for Space Exploration, Science, and Space Operations. Exploration of the Moon and Mars will require advancements in communication systems to manage the demands of the harsh space environment on space electronics, maintain flexibility and adaptability to changing needs and requirements, and provide flexibility and survivability due to increased mission durations. NASA missions can have vastly different transceiver requirements and available resources depending on the science objective, operating environment, and spacecraft resources. For example, deep space missions are often power constrained; operating over large distances, and subsequently have lower data transmission rates when compared to near-Earth or near planetary satellites. These requirements and resource limitations are known prior to launch; therefore, the scalability feature can be used to maximize transceiver efficiency while minimizing resources consumed. Larger platforms such as vehicles or relay spacecraft may provide more resources but may also be expected to perform more complex functions or support multiple and simultaneous communication links to a diverse set of assets.

This subtopic seeks advancements in reconfigurable transceiver and component technology, providing flexible, reconfigurable capability while minimizing on-board resources and cost. The use of open standards within the software radio development is desirable while minimizing potential increased resources and inefficiencies. Topics of interest include the development of software defined radios or radio subsystems which demonstrate reconfigurability, flexibility, reduced power consumption of digital signal processing systems, increased performance and bandwidth, reduced software qualification cost, and error detection and mitigation techniques. Complex reconfigurable systems will provide multiple channel and simultaneous waveforms. Areas of interest can be divided as follows:

Signal Waveforms and On-Orbit Reconfiguration

Multiple waveforms and multiple channel support strive to reduce radio count to reduce power consumption of the overall communication system. Tradeoffs in radio count and radio complexity are considered in the analysis. Reconfiguration for software and firmware upgrades shall provide access control, authentication, and data integrity checks for the reconfiguration process. Partial reconfigurable logic allows simultaneous operation and upload of
new waveforms or functions. Upon operator or automated load detection failure, capability to provide access back
to a known, reliable operational state is needed. An automated restore capability ensures the system can revert to
a baseline configuration, thereby avoiding permanent communications loss due to an errant reconfiguration process.
Approaches should minimize size and power consumption for deep space transceivers incorporating fault tolerant,
reprogrammable digital signal processing devices.

Implementations demonstrating the concept function, and benefits of dynamic or distributed on-board processing
architectures to provide maximum reconfigurability and processing capacity are sought. A common processing
system capacity for communications, science, and health monitoring is envisioned.

Demonstration of adaptive modulation and waveform recognition techniques are desired to provide capability to
reconfigure to the waveform identified based on an on-board library or enable new waveform upload to the on-
board library from the ground.

Software Architecture, Implementation, Modeling and Verification

Development and demonstration of low overhead, low complexity hardware and software architectures to enable
software component or design reuse, or common testing standards that demonstrates cost or time savings.
Emphasis on the application of open standards architecture to facilitate interoperability among different vendors to
minimize the operational impact of upgrading hardware and software components.

Methods (i.e., Hardware Abstraction Layers) that enable portability among reconfigurable logic hardware devices
among different vendors, different device families and types of digital processing technologies.

As the use of software and firmware increases with more flexible and portable software defined radio technologies,
methods are sought to reduce the complexity and cost to space qualify and verify software operation for use in
space yet maintain or increase on-orbit reliability.

Techniques to ensure reliable software execution and failure detection and self-correction.
One promise of software defined radios is software and design reuse maintained in a common repository. The cost or ability to reuse software depends on implementation, development practices, code complexity and other circumstances. This subtopic seeks the development and demonstration of software tools or tool chain methodologies to enable both design and software code reuse.

The Space Telecommunications Radio System (STRS) architecture incorporates the development of an open architecture for NASA Software Defined Radios for space. The STRS standard includes software/firmware and hardware compliance rules that must be followed to comply with the standard. A tools suite that autonomously implements accurate and repeatable tests is required to verify infrastructure, waveform, and hardware STRS compliance. The tool suite must be extendable as the STRS architecture expands to incorporate additional requirements. Innovative solutions are sought under this solicitation to develop the requirements, top level design objectives, and top level design of the compliance tools. The recommended solutions must not incorporate proprietary products or solutions.

Fault Tolerance

The use of reconfigurable logic devices in software defined radios is expected to increase in the future to provide reconfigurability and on-orbit flexibility for waveforms and applications. As the densities of these devices continue to increase and feature size decreases, the susceptibility of the electronics to single event effects also increases. Novel approaches to mitigate single event effects caused by charged particles are sought that reduces power consumption and complexity compared to traditional approaches (i.e., voting schemes and constant updates (scrubbing)).

Techniques and implementations to provide a core waveform capability within the software defined radio in the event of failure or disruption of the primary waveform and/or system hardware. Communication loss should be detected and core or "gold" waveform automatically executed to provide control access to the diagnostic system and over-the-air reload operational waveform and control software.

Radio Architectures

Innovative solutions to provide software defined radio implementations to reduce power consumption and mass. Solutions should promote modularity and common, open interfaces.

Software defined radio implementations that enable future hardware scalability among different mission classes (e.g., low rate deep space to moderate or high rate near planetary, or relay spacecraft). Operational characteristics range from 1's to 10's Mbps at UHF and S-band frequency bands up to 10's to 100's Mbps at X, and Ka-band frequency bands.
Component Technology

Advancements in analog-to-digital converters or digital-to-analog converters to increase sampling and resolution capabilities while reducing power consumption.

Novel techniques to advance memory densities, reduce power consumption, and improve performance in harsh environments.

Advancements in reconfigurable logic technology including processing advancements, radiation hardened commercial technology and advancements in advanced computing such as polymorphous computing.