NASA SBIR 2005 Phase I Solicitation

O1.06  Reconfigurable/Reprogrammable Communication Systems

Lead Center: GRC

Participating Center(s): GSFC, JPL, JSC, MSFC

NASA seeks novel approaches in reconfigurable, reprogrammable communication systems to enable the vision of Space, Exploration, Science, and Aeronautical Systems. Exploration of Martian and lunar environments will require advancements in communication systems to manage the demands of the harsh space environment on space electronics, maintain flexibility and adaptability to changing needs and requirements, and provide flexibility and survivability due to increased mission durations. NASA missions can have vastly different transceiver requirements (e.g. 1’s to 10’s Mbps at UHF and S-band frequency bands up to 10’s to 1000’s Mbps at X, and Ka-band frequency bands.) and available resources depending on the science objective, operating environment, and spacecraft resources. For example, deep space missions are often power constrained; operating over large distances, and subsequently have lower data transmission rates when compared to near-Earth or near-planetary satellites. These requirements and resource limitations are known prior to launch; therefore, the scalability feature can be used to maximize transceiver efficiency while minimizing resources consumed. Larger platforms, such as vehicles or relay spacecraft, may provide more resources but may also be expected to perform more complex functions or support multiple and simultaneous communication links to a diverse set of assets.

This solicitation seeks advancements in reconfigurable transceivers and associated component technologies. The goal of the subtopic is to provide flexible, reconfigurable communications capability while minimizing on-board resources and cost. Topics of interest include the development of software-defined radios or radio subsystems that demonstrate reconfigurability, flexibility, reduced power consumption of digital signal processing systems, increased performance and bandwidth, reduced software qualification cost, and error detection and mitigation technologies. Complex reconfigurable systems will provide multiple channel and multiple and simultaneous waveforms. Areas of interest to develop and/or demonstrate are as follows:

- Advancements in bandwidth capacity, reduced resource consumption, or adherence to standard and open hardware and software interfaces. Techniques should include fault tolerant, reliable software execution, reprogrammable digital signal processing devices;
- Reconfigurable software and firmware that provide access control, authentication, and data integrity checks of the reconfiguration process including partial reconfiguration, which allows simultaneous operation and upload of new waveforms or functions;
- Operator or automated reconfiguration, or waveform load detection failure, and the ability to provide access
back to a known, reliable operational state. An automated restore capability ensures the system can revert
to a baseline configuration, thereby avoiding permanent communications loss due to an errant
reconfiguration process or logic upset;

- Dynamic or distributed on-board processing architectures to provide reconfigurability and processing
capacity. For example, demonstrate technologies to enable a common processing system capacity for
communications, science, and health monitoring;

- Adaptive modulation and waveform recognition techniques are desired to enable transceivers to exchange
waveforms with other assets automatically or through ground control;

- Low overhead, low complexity hardware and software architectures to enable hardware or software
component or design reuse (e.g., software portability) to demonstrate cost or time savings. Emphasis is on
the application of open standard architectures to facilitate interoperability among different vendors and to
minimize the operational impact of upgrading hardware and software components;

- Software tools or tool chain methodologies that enable both design and software modeling and code reuse,
and advancements in optimized code generation for digital signal processing systems;

- The use of reconfigurable logic devices in software-defined radios is expected to increase in the future to
provide reconfigurability and on-orbit flexibility for waveforms and applications. As the densities of these
devices continues to increase, and size decreases, the susceptibility of the electronics to single event
effects also increases. Novel approaches are sought to mitigate single event effects in reconfigurable logic
cauised by charged particles, thereby improving reliability. New methods may show advancements in
reduced cost, power consumption, or complexity compared to traditional approaches (i.e., voting schemes
and constant updates (e.g., scrubbing)).

- Techniques and implementations to provide a core capability within the software-defined radio in the event
of failure or disruption of the primary waveform and/or system hardware. Communication loss should be
detected and core capability (e.g., "gold" waveform code) is automatically executed to provide access
control and restore operation;

- Innovative solutions to software-defined radio implementations that reduce power consumption and mass.
Solutions should enable future hardware scalability among different mission classes (e.g., low-rate, deep
space to moderate or high-rate near planetary, or relay spacecraft) and should promote modularity and
common, open interfaces; and

- In component technology, advancements in analog-to-digital converters or digital-to-analog converters to
increase sampling and resolution capabilities; novel techniques to increase memory densities; and
advancements in processing and reconfigurable logic technology, each reducing power consumption and
improving performance in harsh environments.